UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,777	08/16/2002	Hsin-Ta Lee	CMOP0023USA	2572

27765 7590 05/07/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
LABAZE, EDWYN	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,777	LEE ET AL.	
	Examiner	Art Unit	
	EDWYN LABAZE	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of amendments filed 2/21/2004.

2. Claims 1-43 are presented for examination.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanai et al. (U.S. 5,369,512).

Re claim 1: Yanai et al. discloses active matrix liquid crystal display with variable compensation capacitor, which includes [two substrates] an upper substrate, a lower substrate, and a plurality of pixels [herein Yanai et al. defines a pixel as a thin film transistor/TFT see col.1, lines 10+] located between the upper substrate and the lower substrate, each of the pixels having at least a [variable] compensating capacitor 6 [herein as shown in figs. # 5-6; Yanai et al. teaches that the variable compensation capacitor compensates (i.e. means of offsetting, equalizing) the potential/voltage fluctuation, therefore providing identical voltage through each

pixel] for providing an approximately identical feed-through voltage for each of the pixels (col.7, lines 40-67).

Re claims 2 and 23: Yanai et al. teaches an apparatus, further comprising a first scanning line 11, a second scanning line 12, and a scanning line driving circuit 4, each of the pixels/TFT 2 being located between the first scanning line 11 and the second scanning line 12, each of the first scanning line and the second scanning line having a first input end so that the scanning line driving circuit can input signals into the first scanning line and the second scanning line through the first input ends (see fig. # 6 of Yanai et al.; col.8, lines 8+).

Re claims 3, 6, 11, and 39: Yanai et al. discloses an apparatus, wherein a capacitance of each of the compensating capacitors is increased when a distance [herein disclosed as a time period] between the pixels and the first input end of the second scanning line is increased (col.7, lines 15-67).

Re claim 4: Yanai et al. teaches an apparatus, further comprises a liquid crystal cell 84 having a common electrode, a pixel/TFT electrode 83 connected to the corresponding compensating capacitor, and a liquid crystal layer disposed between the pixel electrode and the common electrode; and a thin film transistor 83 having a gate electrode 85 connected to the first scanning line, a drain electrode 86 connected to a corresponding first data line, and a source electrode 86 connected to the pixel electrode (as shown in fig. # 1 of Yanai et al.; col.5, lines 22-40; col.6, lines 47-60).

Re claims 5, 13, and 20-21: Yanai et al. discloses an apparatus, wherein each of the compensating capacitors 6 is composed of a first overlapping region S1, which is formed by

overlapping the corresponding pixel electrode over the first/second/third scanning line (col.3, lines 6-19; col.10, lines 10-25).

Re claims 14, 24-25, and 36: Yanai et al. discloses an apparatus, wherein an area of each of the first overlapping region S1 is increased as a distance between the second input end and the pixel, corresponding to each of the first overlapping regions is increased (as shown in fig. # 8 of Yanai et al.; col.9, lines 55-67; col.10, lines 1+).

Re claims 7, 15, and 26: Yanai et al. teaches an apparatus, wherein each of the compensating capacitor 6 is composed of a second overlapping region S2, which is formed by overlapping the corresponding source electrode over the corresponding gate electrode (col.10, lines 26+).

Re claims 8, 16, 28-29, and 37: Yanai et al. discloses an apparatus, wherein an area each of the second overlapping regions is increased as a distance between the first input end of the first scanning line and the pixel corresponding to each of the second overlapping regions is increased (col.10, lines 38+).

Re claims 9, 17, and 41-43: Yanai et al. teaches an apparatus, further comprises a storage capacitor, and a capacitance of each of the storage capacitors is reduced as a distance between each of the storage capacitors and the first input end of the second scanning line is increased (col.6, lines 7+).

Re claim 10: Yanai et al. discloses an apparatus, further comprising a second data line [herein Yanai et al. discloses a plurality of stripe-like data bus lines 5] and a data line driving circuit, each of the pixels/TFT 2 being connected to the second data line, which has a second

input end so that the data line driving circuit can input signals into the second data line through the second input end (see fig. # 3 of Yanai et al.; col.6, lines 40+; col.7, lines 35+).

Re claim 12: Yanai et al. teaches an apparatus, wherein each of the pixels is located between a third scanning line and a fourth scanning line [Yanai et al. teaches a plurality of scanning bus lines 11 & 12, and each pair of scanning lines 11 & 12 are arranged in parallel formation on each side of the corresponding reference potential 4 as shown in fig. # 6; col.8, lines 10+], and further comprises: a liquid crystal cell 84 having a common electrode 88, a pixel electrode 83 connected to the corresponding compensating capacitor 6, and a liquid crystal layer [disclosed by Yanai et al.; but not shown see col.5, lines 25] disposed between the pixel electrode and the common electrode 88; and a thin film transistor 83 having a gate electrode 85 connected to the corresponding third scanning line, a drain electrode 86 connected to the second data line, and a source electrode 86 connected to the pixel electrode (as shown in fig. # 1 of Yanai et al.; col.5, lines 22-40; col.6, lines 47-60).

Re claim 18: Yanai et al. discloses an apparatus comprising, a plurality of scanning lines 11 & 12; a plurality of data lines 5; and a plurality of pixels/TFT 2, each of the pixels having a pixel electrode 84a, and a thin film transistor 83 having a gate electrode 85 connected to the corresponding scanning line 11/12, a drain electrode 86 connected to the corresponding data line 5, and a source electrode 86 connected to the pixel electrode (col.5, lines 25+), wherein a first overlapping region S1 is formed by overlapping the pixel electrode over the corresponding scanning line 11/12; wherein an area of each of the first overlapping regions is increased gradually along a first direction (as shown in fig. # 8 of Yanai et al.; col.11, lines 35+).

Re claims 19 and 27: Yanai et al. teaches teaches an apparatus, wherein each of the first overlapping region forms a compensating capacitor 6 for providing an approximately identical feed-through voltage for each of the pixels, thus reducing a flicker [to one skilled in the art, a flicker phenomenon is induced in vertical lines due to electrical cross talk between liquid crystal cell arranged along the data lines. Therefore, Yanai et al. means of reducing the flicker effect] effect of the liquid crystal display panel (col.7, lines 50-67; col.12, lines 58+; col.13, lines 50-67).

Re claim 22: Yanai et al. discloses an apparatus, wherein a protrusion structure is disposed on each of the pixel electrodes and above the corresponding second extending portion, for regulating an alignment [such as a planar] direction of the liquid crystal molecules (col.11, lines 25+).

Re claims 30 and 34: Yanai et al. discloses an apparatus, comprising a scanning line driving circuit 4; a data line driving circuit; at least a data line [from a plurality of data lines 5] connected to the data line driving circuit; at least a scanning line 11/12 connected to the scanning line driving circuit 4; a first region S1 positioned on the scanning line 11/12 having at least a first pixel 2, which comprises a first pixel electrode 3 (see fig. # 6 of Yanai et al.), a first overlapping region being formed by overlapping the first pixel electrode over the scanning line (col.), lines 9-25); and a second region S2 positioned on the scanning line 11/12 having at least a second pixel, which comprises a second pixel electrode, a second overlapping region being formed by overlapping the second pixel electrode over the scanning line (col.10, lines 26+); wherein the first region is located between the scanning line driving circuit and the second region, and an

area of the second overlapping region is larger than an area of the first overlapping region (col.11, lines 1-44).

Re claims 31-32: Yanai et al. teaches an apparatus, wherein the first pixel [herein disclosed as P.sub.i] further comprises a first thin film transistor 2, which includes a first gate electrode connected to the scanning line 11/12, a first drain electrode 122 connected to a first data line, and a first source electrode 121 connected to the first pixel electrode, and a third overlapping region [which is formed due to different capacitance from the lower electrode to the upper and from one pixel to another one] is formed by overlapping the first source electrode over the first gate electrode 109, 164 (as see in figs. # 13-16 of Yanai et al.; col.8, lines 25-52; col.13, lines 8+).

Re claims 33 and 35: Yanai et al. discloses an apparatus, wherein an area of the fourth overlapping region is larger than an area of the third overlapping region [since the pixel electrodes are arranged in pair and continuous pattern, therefore the odd overlapping regions are identical and similarly for the even overlapping regions. As proven above, wherein the second overlapping region is larger than the first overlapping region, the same is true for the fourth and third overlapping regions] (col.11, lines 1-44).

Re claim 38: Yanai et al. teaches an apparatus, a plurality of scanning lines 11, 12 for transmitting scanning signals from a scanning line driving circuit 4; a plurality of data lines 5 for transmitting image signals from a data line driving circuit; and a plurality of pixels (as shown in fig. # 19 of Yanai et al.; col.16, lines 50+), each of the pixels comprising: a liquid crystal capacitor [as defined by two conductive layers separated by a thin dielectric layer] (col.); a thin film transistor 2 electrically connected to the corresponding scanning line 11/12 the

corresponding data line 5 (col.16, lines 50+), and the liquid crystal capacitor a compensating capacitor 306 electrically connected between the liquid crystal capacitor and the corresponding scanning line 11/12, being connected to the thin film transistor 2, for providing an approximately identical feed-through voltage for each of the pixels (col.16, lines 55+).

Re claim 40: Yanai et al. discloses an apparatus, wherein a capacitance of each of the compensating capacitors is increased as a distance between the pixels and the data line driving circuit is increased (col.7, lines 15-67).

Response to Arguments

6. Applicant's arguments with respect to claims 1-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ueda et al. (U.S. 5,459,596) teaches active matrix liquid crystal display with supplemental capacitor line, which overlaps signal line.

Sukegawa et al. (U.S. 5,546,205) discloses active matrix liquid crystal display panel having compensating capacitor provided without lowering pixel aperture ratio.

Mori et al. (U.S. 5,668,650) teaches thin film transistor panel having an extended source electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (571) 272-2395. The examiner can normally be reached on 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

el
Edwyn Labaze
Patent Examiner
Art Unit 2876
April 21, 2004